

09/195,473

**REMARKS**

This Application continues the prosecution of the claims which were not allowed in the parent Application.

The Amendment of December 5, 200, filed in the parent Application Serial No.: 09/195,473, was not entered in its entirety.


Claims 7 and 8 are substituting Claims 1 and 2 of the parent Application with changes to reflect the comments in the Advisory Action. These amendments were not previously entered as raising new issues and requiring a further search.

The Claims no longer state that the oscillator "generates" the first and second signals.

Favorable reconsideration is respectfully requested.

Attached hereto is a marked-up version of the changes to the Claims captioned "Version with Markings to Show Changes Made." The deleted subject matter is shown in brackets and the added subject matter is underlined.

Respectfully submitted,  
SCHULTE, ROTH & ZABEL, LLP  
Attorneys for Applicants  
919 Third Avenue  
New York, New York 10022  
(T) 212-756-2000  
(F) 212-593-5955

By   
Donna L. Angotti  
Reg. No. 32,679

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a first current mirror circuit comprising a third and a fourth MOS transistors of a second conductivity type each having a source, a drain and a gate, the drains of said third and fourth MOS transistor being connected to the drains of said first and second MOS transistors, respectively, the gates of the third and fourth MOS transistors connected to each other and the gate and drain of said third MOS transistor;

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a fifth MOS transistor of the second conductivity type having a source, a drain and a gate, and receives the first signal at the gate thereof;

a sixth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the second signal at the gate thereof;

a second current mirror circuit comprising a seventh and an eighth MOS transistors of the first conductivity type each having a source, a drain and a gate, the drains of said seventh and eighth MOS transistors being connected to the drains of said fifth and sixth MOS transistors, respectively, the gates of the seventh and eighth MOS transistors being connected to each other and the gate and drain of said seventh MOS transistor being connected; and

an output buffer circuit for generating an output signal based on a signal generated at the drain of said fourth MOS transistor and a signal generated at the drain of said eighth MOS transistor.

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